

DEVELOPMENT OF A HIGH EFFICIENCY  
THIN SILICON SOLAR CELL

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Second Quarter Progress Report

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by

Joseph Lindmayer, et al

SOLAREX CORPORATION

1335 Piccard Drive

Rockville, MD 20850

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# TECHNICAL CONTENT STATEMENT

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## I. ABSTRACT

The present contract has reached the stage of two-thirds completion. Progress can be characterized by continuous improvement in all parameters of this new space cell. The CHEVRON<sup>1</sup> metalization pattern is efficient in collecting the current and a special titanium-silver metalization provides high reliability contacts. The cells made to date primarily employ evaporated tantalum oxide coatings, which can now be applied quite reproducibly. The cells display extremely sharp I-V characteristics and high photovoltages. The blue response has also been improved significantly. In general, the efficiencies have been gradually improved throughout the period.

So far, only modest attention has been paid to the red response of the cell. Efforts in the last quarter will concentrate on improving the rear high-low junction properties and on implementation of an internal mirror.

It appears certain that the project will demonstrate a space solar cell having a new technological basis. Additional performance will also very likely be achieved through improvements in the red response. It appears that the new technological basis developed during this contract warrants further "fine tuning" of the processing in order to maximize the conversion efficiency and to use the present technology to its fullest potential.

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### III. INTRODUCTION

The aim of this contractual effort is to attempt realization of higher specific power output and radiation resistance from thinner solar cells for space applications. The work reported herein describes the efforts applied to establishing the technological base for fabricating high efficiency thin solar cells. The contractual period has reached the two-thirds point and achievement of the goals now appears a certainty.

The efforts expended in this project have been divided into some nine categories in the development of this new space cell. These cells are  $n^+p$  in form and the front  $n^+p$  junction formation has employed phosphorus as the dopant from a gaseous  $PH_3$  source. The  $p^+p$  high-low junction on the back has been fabricated by alloy/diffusion of an aluminum layer applied by vacuum evaporation, which requires further study to optimize recombination site densities. Cells have been processed with starting resistivity silicon of 0.2-3 ohm-cm, but the low-resistivity cells require further effort to achieve reproducible surface properties. Crystal orientations employed have been (100) and (111), with the former resulting in decreased fill-factor scatter. Anti-reflection coatings for improving optical coupling of the incident light have mostly been evaporated tantalum oxide, with some titanium dioxide and yttrium oxide experimental coatings. Cells were successfully fabricated from

silicon of various thicknesses, from 11 mils down to 4 mils, resulting in power and current reductions of only 17% for thickness reductions by a factor of 2.5. Assessment of processing rate limitations for very thin silicon cells shows that manual transfer steps presently require more care to avoid breakage, but some improvements have been considered. Some calculations of theoretical limitations on cell photovoltage have been performed, including effects from distributions of photogenerated carriers. In addition, for analytical support on these efforts, modifications and improvements to optical and electronic measurement instrumentation and mathematical analysis aids have been made during this quarter.

#### IV. TECHNICAL DISCUSSION

Efforts during the second quarter resulted in completion of several tasks and significant progress in the continuing tasks. Modification and improvement of measurement apparatus was completed for AM0 simulation, I-V, C-V, lifetime, and quantum yield vs. wavelength. A supply of 0.2 ohm-cm wafers was obtained and some quantity of 2 cm x 2 cm cells were fabricated. Variations in thickness, starting resistivity and processing techniques have been investigated to determine effects on cell performance. Experimentation with phosphorus diffusion conditions was completed, but back contact experiments continue due to some remaining difficulties with recombination velocity. The cells fabricated from 2-3 ohm-cm starting resistivity are very reproducible, with excellent fill factors and good blue response. The processing techniques employed have resulted in devices of high quality and a very manageable process flow. The main processing rate limiting steps lie in handling and cleaning of thin cells, which do require caution to avoid breakage.

##### A. Front Junction Formation

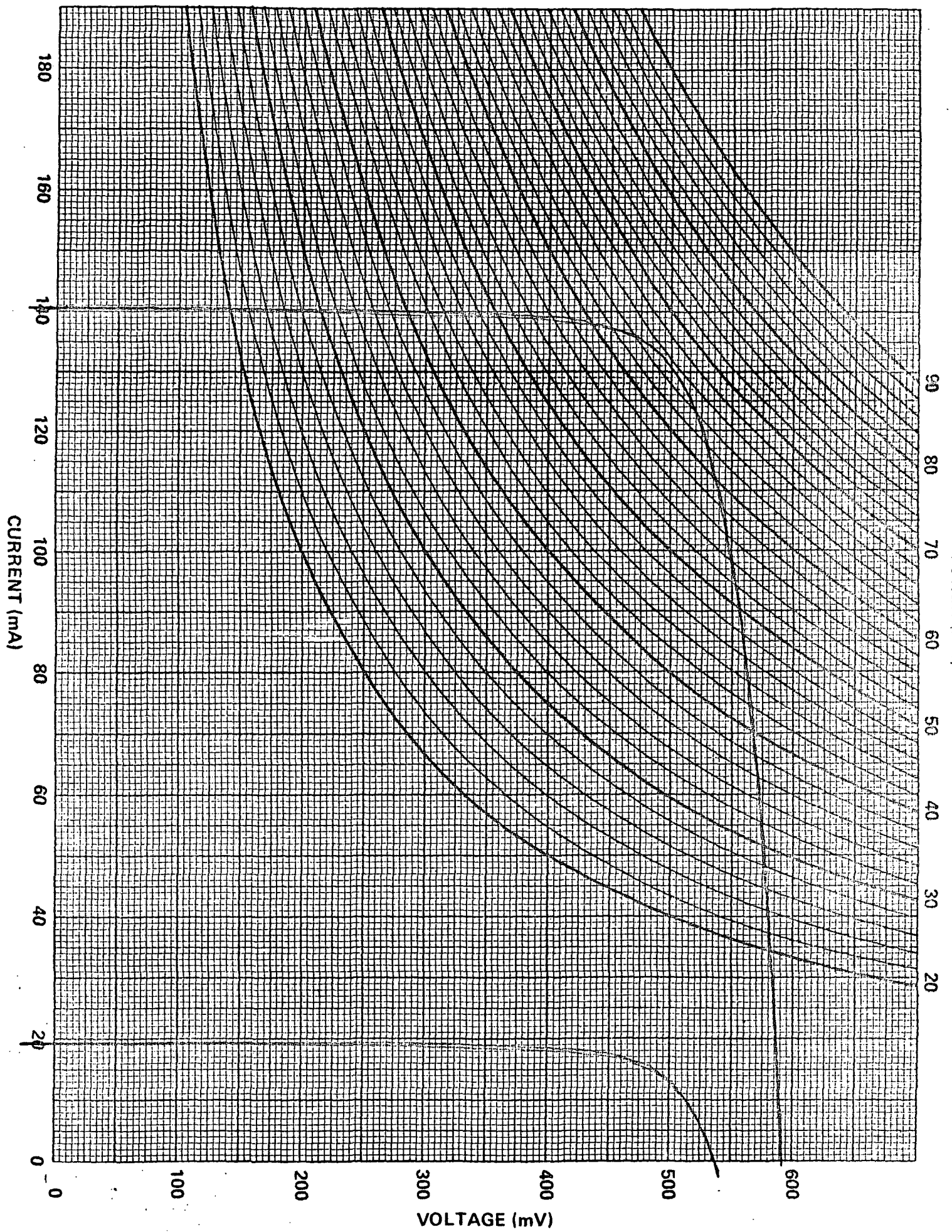
Diffusion of the front junction employed a gaseous source consisting of a mixture of  $N_2$ , Ar,  $O_2$ , and  $PH_3$ . The main variables controlling the diffusion process are the temperature of diffusion, the time at temperature and the gas mixture composition. The desired results are an optimum sheet resistance in the  $n^+$  layer and minimum damage to the silicon crystal lattice. The sheet resistances obtained are quite reproducible, as determined by four-probe measurement, and are set at approximately

100 ohms per square. The degree of lattice damage associated with the diffusion process was evaluated by measurement of the dark forward current characteristics and the forward injection storage capacitance at low current densities, as described in Section J. During the effort on variation of diffusion parameters it became apparent that good fill factors, improved storage times and dark current characteristics were obtained with diffusions performed in the neighborhood of 860°C for 10 minutes, with gas compositions near 1:10:100:100 for  $\text{PH}_3:\text{O}_2:\text{Ar}:\text{N}_2$ . These diffusion conditions have produced 5mA per  $\text{cm}^2$  of short wavelength response below 0.55 micron, using a Corning 9788 glass filter in the AM0 simulator path, as shown in Figure 1. for a 10 mil thick cell.

#### B. Back High-Low Junction Formation

As mentioned in earlier reports, the system being investigated in this effort for forming a high-low junction at the rear surface of the cells is the diffusion/alloying of aluminum. In most cases, the aluminum was applied by evaporation and alloyed through the rear phosphorus junction. The aluminum-silicon eutectic temperature is known to be at 577°C, while considerable aluminum penetration is well known to occur down to around 450°C. At higher temperatures, the aluminum easily penetrates and overwhelms the pre-existing  $\text{n}^+\text{-p}$  phosphorus doped junction. Above 660°C the aluminum itself goes into the liquidus phase and the whole sandwich of back layers re-solidifies on cooling. The properties of the high-low junction are then determined by the net stress and doping of the former eutectic interface and the





associated diffusion front. The interfacial recombination velocity resulting from this structure determines the efficiency of reflecting photogenerated electrons toward the front junction for collection. It must be considered that too mild an aluminum penetration would leave an  $n^+$  potential minimum which would force electron motion toward the back surface, but this effect appears to be easily overcome as shown by the data on isochronal (15 min.) alloying temperature experimentation in Figure 2. Higher temperatures of alloying appear to degrade the interfacial recombination velocity, as evidenced by the monotonic decrease in collected current with increasing temperature. However, consistently high photovoltages and the asymptotic increase in collected photocurrent with decreasing alloying temperature down to 650°C indicate no problem in overcoming the prior  $n^+$  layer.

The resultant recombination velocity appears to be higher than hoped and a function of detailed metallurgy, as shown by the scatter in long wavelength yield in Figure 3. (The measurement technique is described in Section J.) Concerted efforts continue to be directed to improvement of carrier lifetime at the back interface, but it is obvious that this system will require further investigation in the immediate future.

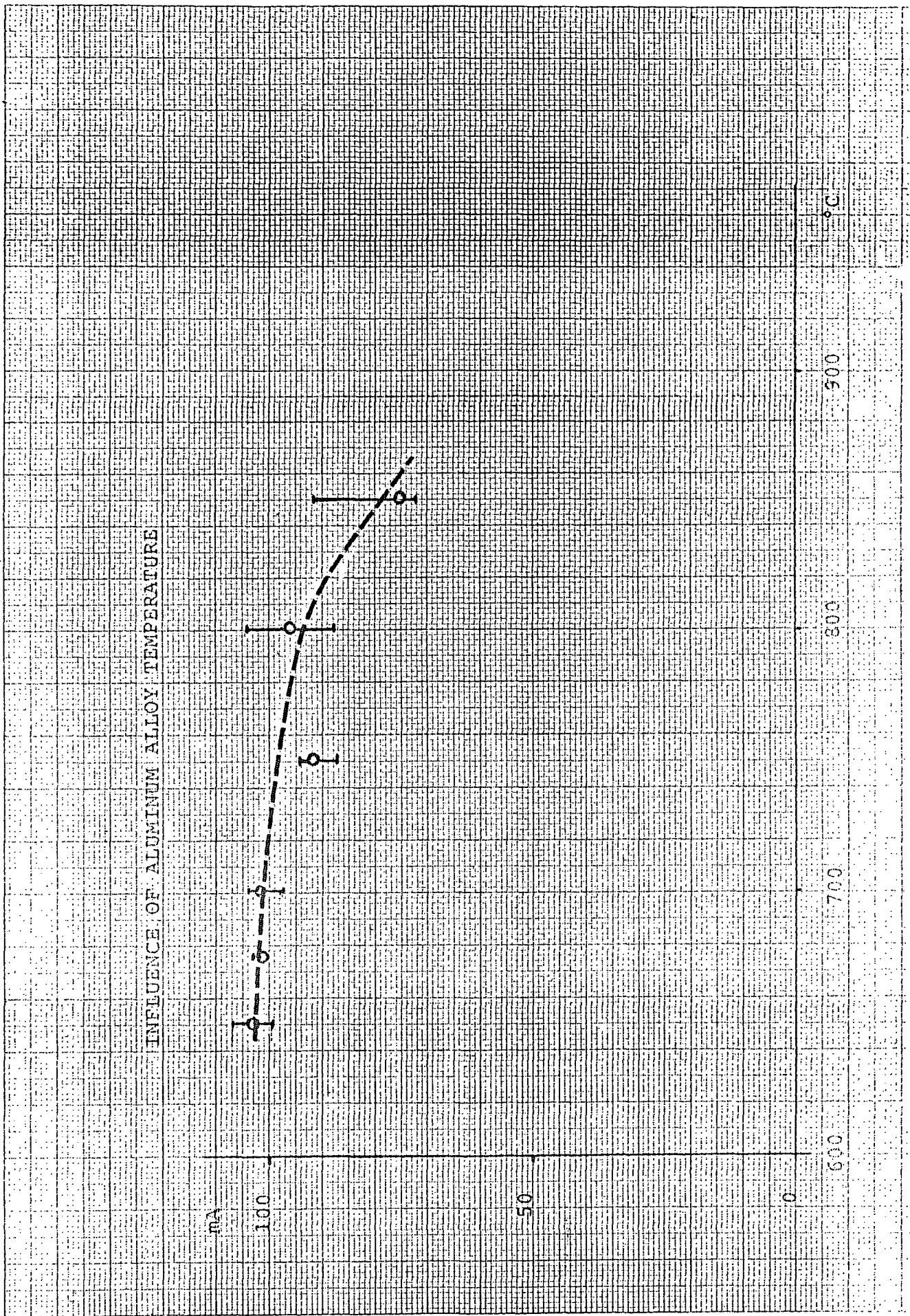
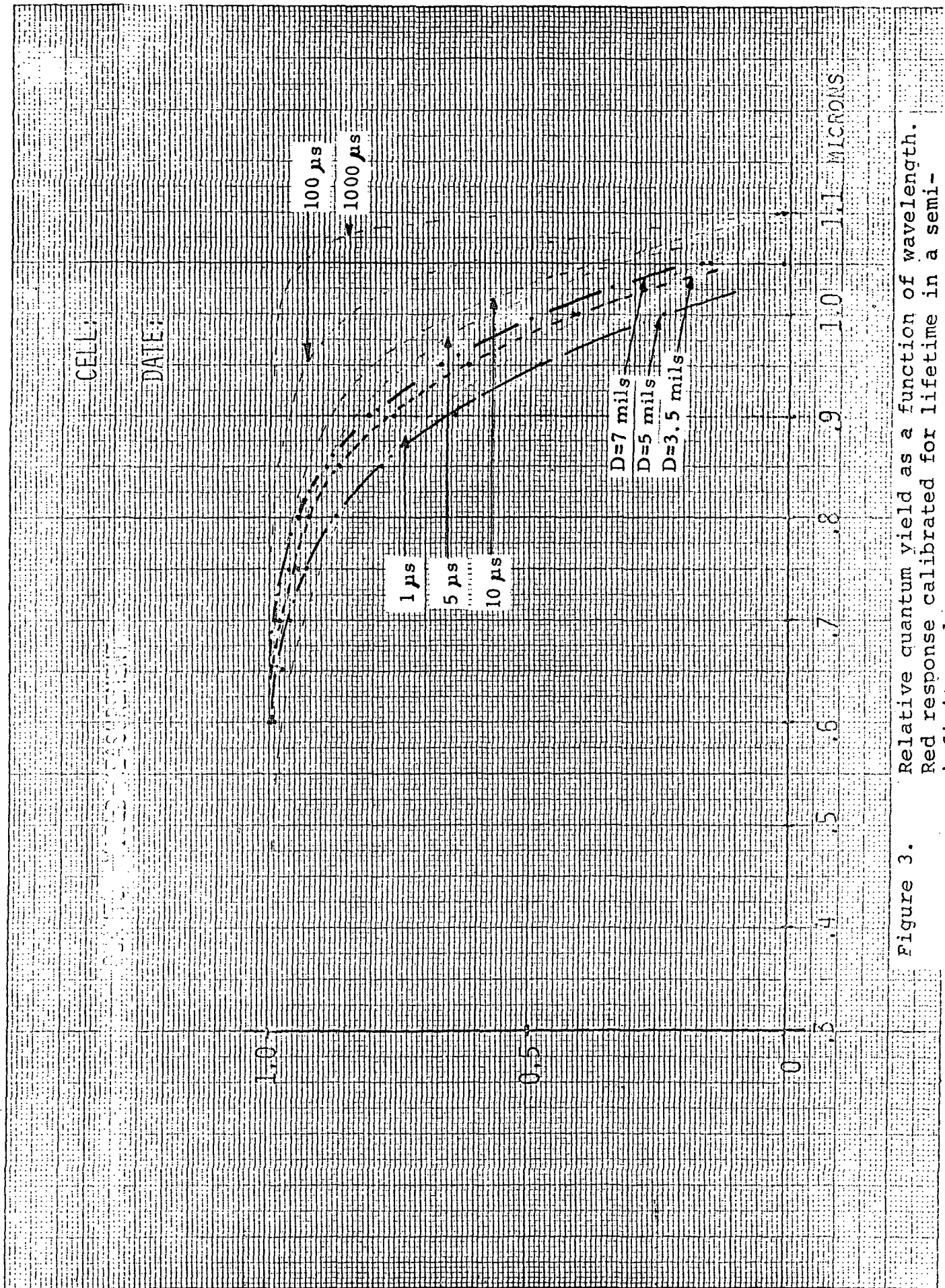


Figure 2. Short-circuit current vs. aluminum alloy temperature (no anti-reflection coating applied) for 2 cm x 2 cm cells.



### C. Low Resistivity Silicon

A supply of p-type wafers of 0.2 ohm-cm resistivity was obtained for use in this effort. Cells were fabricated in much the same fashion as for the 2-3 ohm-cm wafers normally employed. Cell performance was fairly similar except for one outstanding aspect, the variation and instability of the fill factor and photovoltage. This is explained by the decreasing ratio of  $n^+$  to p doping levels, which in very shallow junctions allows increasing interaction of the surface of the  $n^+$  layer with the minority carrier distributions in the neighborhood of the junction. As a consequence, chemical interactions with the ambient, which change the surface state properties, exert increased control over the current-voltage characteristics of the junction. The net result is that the immediate chemical history of the cell surface affects the characteristics of the cell, as can be seen in the dark-current plot in Figure 4. Control of these properties and stabilization of the fill factor for low-resistivity cells represents a level of effort which does not fit within the resources of the present contract funding. Thermal oxidation techniques are well known for stabilizing surface state conditions on silicon, but the oxidation temperatures and resultant oxide thicknesses normally employed are incompatible with low-temperature cell processing and efficient anti-reflection coatings. Certainly, there must be a compromise technology for achieving stable low surface state densities on low resistivity cells in conjunction with



Ampere

Average resistivity 0.2 ohm-cm

$10^{-1}$

$10^{-2}$

$10^{-3}$

$10^{-4}$

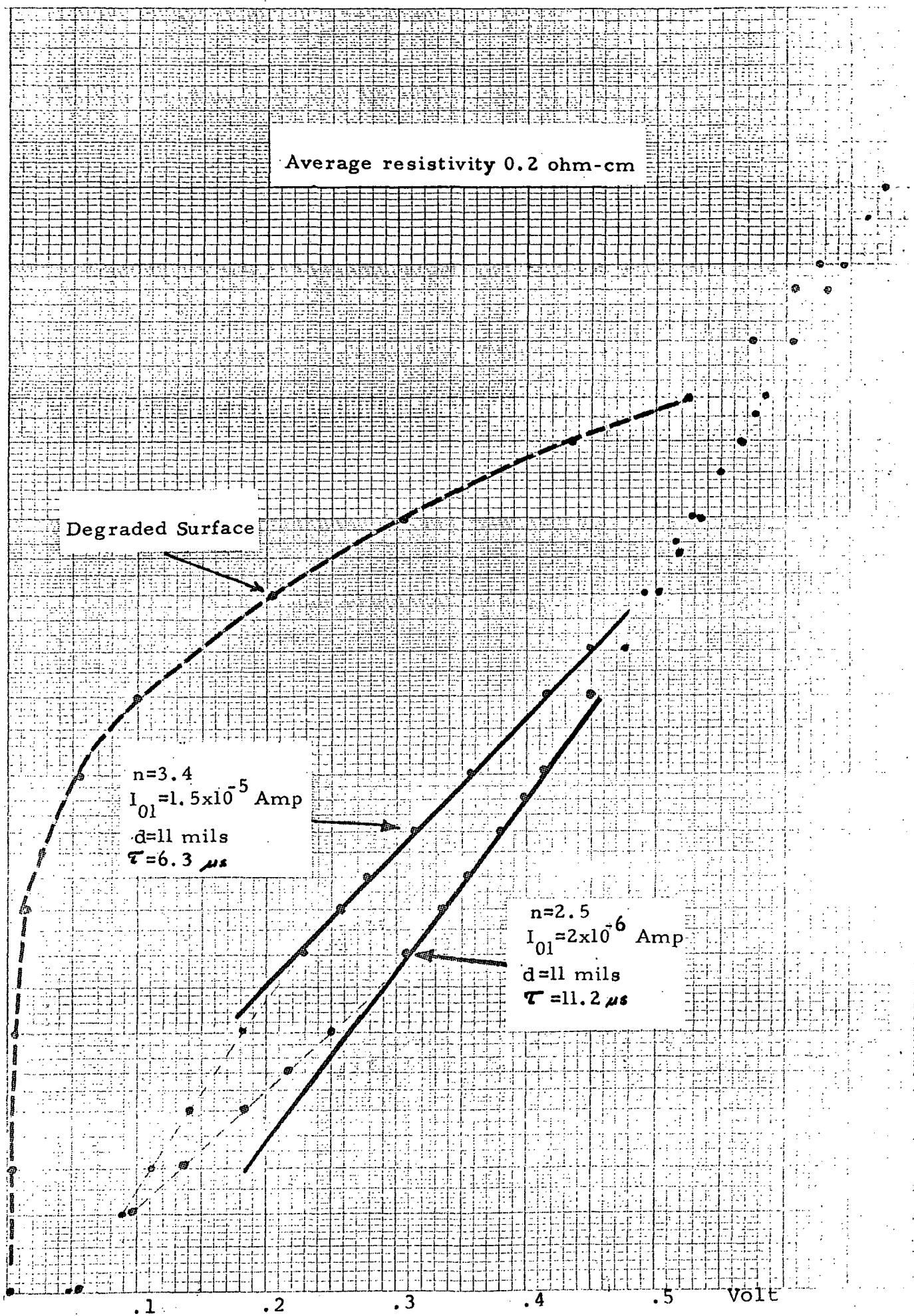
$10^{-5}$

Degraded Surface

$n=3.4$   
 $I_{01}=1.5 \times 10^{-5}$  Amp  
 $d=11$  mils  
 $\tau=6.3 \mu s$

$n=2.5$   
 $I_{01}=2 \times 10^{-6}$  Amp  
 $d=11$  mils  
 $\tau=11.2 \mu s$

Volt



high-index antireflection coatings. We could pursue this subject to successful conclusion in some future efforts.

#### D. Crystal Orientation

In the course of the first two quarters wafers of both (100) and (111) orientation have been employed for solar cell fabrication. In general, the characteristics of cells having the two different surface orientations are remarkably similar, with one exception. The cells fabricated on (100) surfaces were quite reproducible in fill factor, while those employing the (111) orientation scattered quite randomly in fill factor. Devices of equal quality can be made with either orientation, but the yield for the (111) orientation has been consistently lower in our experience.

#### E. Anti-Reflection Coatings

As was reported before, most of the work concentrated around the use of evaporated tantalum pentoxide. It was found that this oxide can provide good transparency even in the ultraviolet region. The index of refraction appears to be a strong function of evaporation conditions, with the general tendency being toward the establishment of a suboxide having an index value below that associated with the amorphous state. The two most important parameters in the evaporation of tantalum oxide appear to be the ambient pressure and the rate of evaporation.

A sufficiently high index of refraction can be developed by evaporating at a high rate at the lowest possible pressure. This anti-reflection coating appears to be under good control, is being applied routinely and no further work will be done on this subject in the oncoming quarter.

Short experimental excursions were made in the direction of employing yttrium oxide as an alternate anti-reflection coating. This oxide appears to have most of the desired properties and also shows changes in the index of refraction related to the evaporation conditions. Figure 5. shows a typical reflection curve obtainable by the application of yttrium oxide. Work in this direction was stopped, however, as the scope of this effort does not allow the full exploration of this oxide.

Another search for a better optical match consisted of the application of double layers. Particularly, we used a thin layer of titanium metal coated with evaporated tantalum oxide. Upon heating in air, in the neighborhood of 500°C, the titanium layer became oxidized to form  $\text{TiO}_2$ . It was discovered, however, that titanium has peculiar oxidation properties in that the oxidation rate is a strong function of evaporation condition history. Nevertheless, successful double layers were applied and an improvement in the optical match was observed following addition of a cover slide. This



is shown in Figure 6. The observed passband widening of the optical transmission is due to the higher index displayed by the underlying  $\text{TiO}_2$  layer. Again, detailed mapping of this system has been terminated because of effort limitations.

The use of evaporated tantalum oxide appears to produce sufficiently good optical coupling for the moment and will be employed in the oncoming quarter.

#### F. Thin Cells

Groups of experimental 2 cm x 2 cm cells were fabricated during this quarter in silicon of various thicknesses, utilizing the best-case combination of the processing techniques described above. The silicon thickness was varied in approximately one mil steps from 11 mils down to 4 mils, employing 2 to 3 ohm-cm (100) silicon starting material. The resulting AM0 cell performance of the groups of devices fabricated is shown in Figure 7. and Figure 8. along with data for thick 15 mil cells.

These cells had tantalum oxide anti-reflection coatings at the AM0 measurement step, but no cover glass, which raises the output about 5%. As expected, the short-circuit current is a slow function of thickness; losing only the long wavelength photocurrent in the deep bulk as the thickness is decreased. The peak power curve undergoes the same relative drop as the current, since these devices all have excellent fill factors and the drop in open-circuit photovoltage with decreasing cell

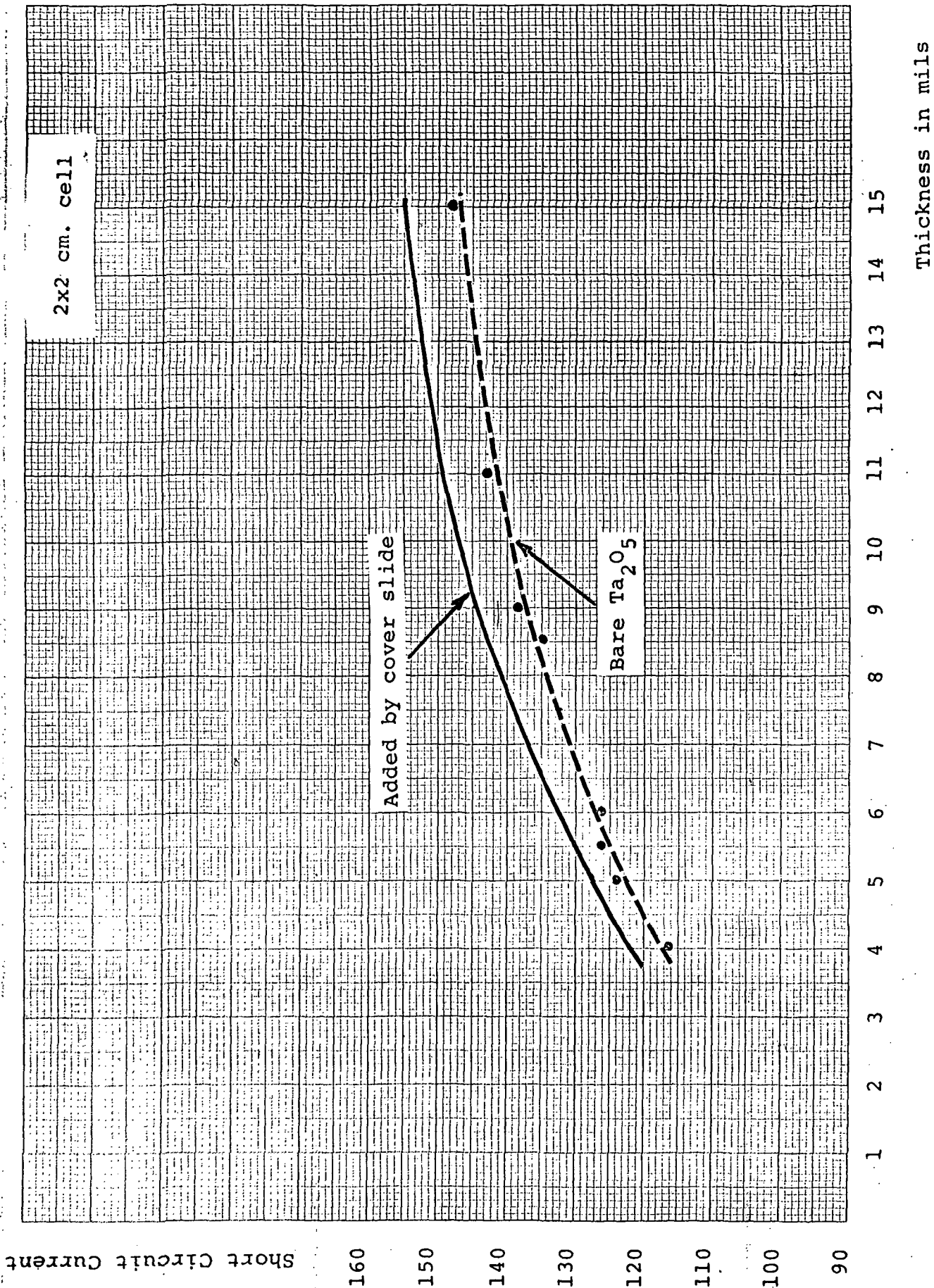


Figure 7. Present status of short-circuit current vs. cell thickness for 2-3 ohm-cm cells.

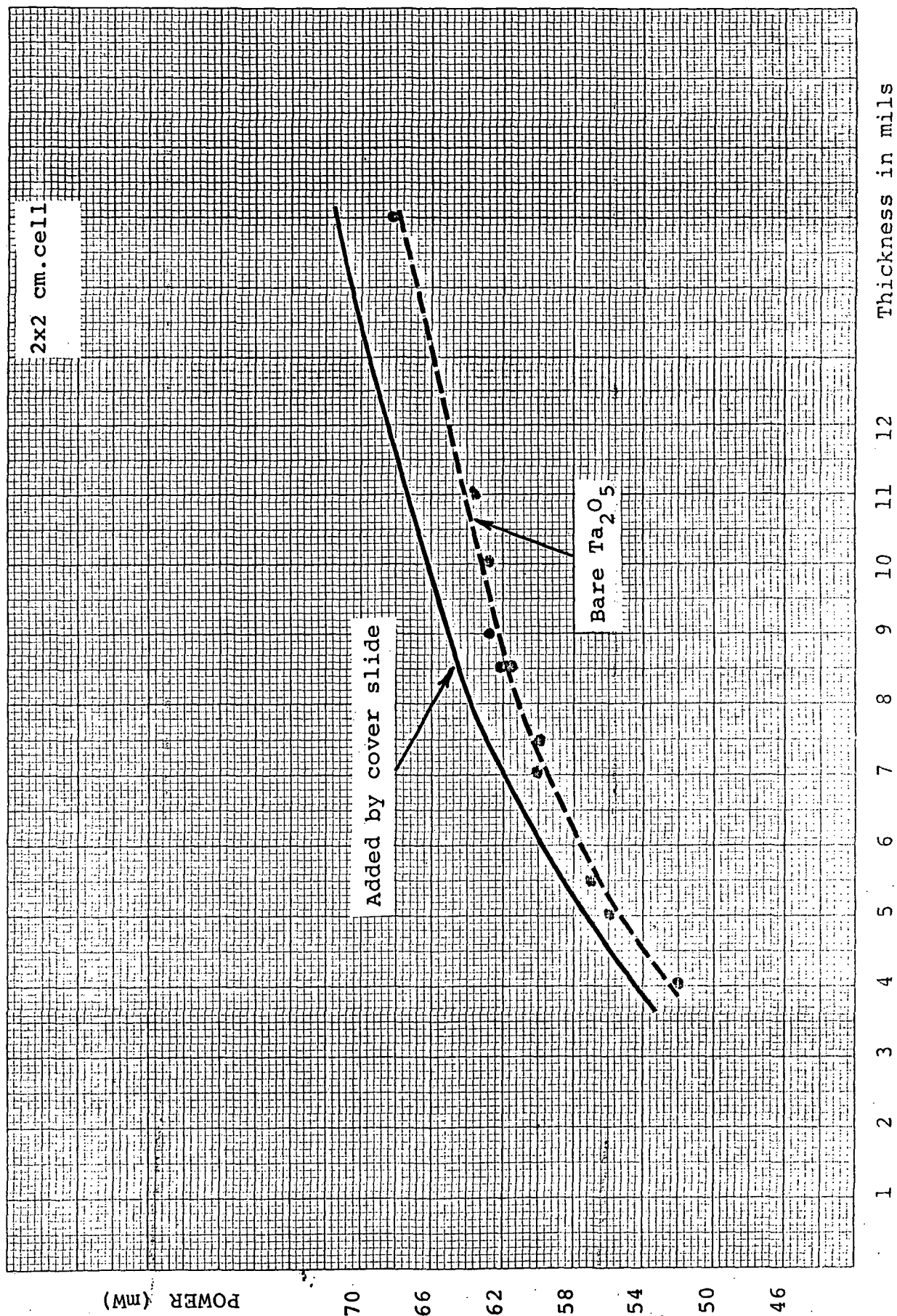


Figure 8. Present status of maximum power vs. cell thickness

thickness was very small. Reducing the cell thickness by a factor of 2.5 from the common 10 mil starting material only reduces the AMO output current by 17%, a significant improvement in power to weight ratio.

#### G. Processing Rate Limiting Steps

The processing technology employed for these experimental cells at Solarex is very tractable and will lend itself well to high-rate fabrication. We firmly believe that a pilot-line level of fabrication would be most useful for fine tuning of the various steps to maximize performance. The main rate limiting steps now appear to lie in handling and cleaning of the more fragile thin silicon. No problems were encountered with thinner silicon in high-temperature steps, but rather in the manual transfer stages. The most fruitful processing rate improvement for thin cells lies in the equipment methodology for handling and holding devices. Venturi-tweezer pickups and low-force jigging for drying and evaporator mounting, would reduce the great care and time consumption presently required in these steps. The other processing steps lend themselves well to high-rate batch or continuous-flow operations with no particular precautions required for thin cells. All operations could lead to very high throughput rates,

#### H. Photovoltage

The photovoltage of a cell can be related to the theoretical reverse current of the junction. In a mathematical formulation,

thermal generation centers must be identified. If one assumes that the bulk lifetime is relatively high, the source of the reverse current shifts to the boundaries. In such a case, the reverse current components are determined by the appropriate surface recombination velocities. On the back side, the thermal generation centers are determined by the technology employed. While the problem of forming a high-low junction seems almost trivial, the actual technology employed will determine the density of thermal generation states introduced into the lattice. (This factor also relates to the red response of the cell.) At the front junction, the surface recombination velocity is determined by the heavily doped portion of the diffused layer involving the first few hundred angstroms. When one has a junction that is only a couple of thousand angstroms deeper into the silicon, the reverse current component of the front layer is defined. Numerical calculations will show that for bulk resistivities less than 1 ohm-cm, this component dominates. The photovoltage associated with these limitations is approximately 600 mV at one sun.

It has been recognized for some time that a photovoltage contribution arises from the rear high-low junction for lightly doped substrates. However, in order to increase the photovoltage

significantly above 600 mV, the details of the front junction must be better understood. Clearly, this reverse current component is a delicate function of the details of the impurity concentrations and profiles. Experimental excursions into this area (using 0.2 ohm-cm substrates) indicates a basic instability. More precisely, the photovoltage and the fill factor become a function of the precise surface treatment such as chemical cleaning, type of AR coating, temperature treatments, etc. It appears certain now that an entirely new set of parameters enter into the situation. Concerted exploration into this new area has not been done in the past.

We expect a better definition of the problem by the final report. Increased understanding of this problem would result in a gradually improving photovoltage.

#### J. Electrical Analysis Measurements

The physical properties of cells fabricated in the course of this project were analyzed by both optical and electronic techniques to determine the effects of experimental alterations of the processing technology. Measurement of photovoltaic conversion performance under calibrated AM0 conditions in the simulator does not lend sufficient insight into the operation of the various component portions of the cells. Consequently, measurements are also performed to evaluate optical coupling

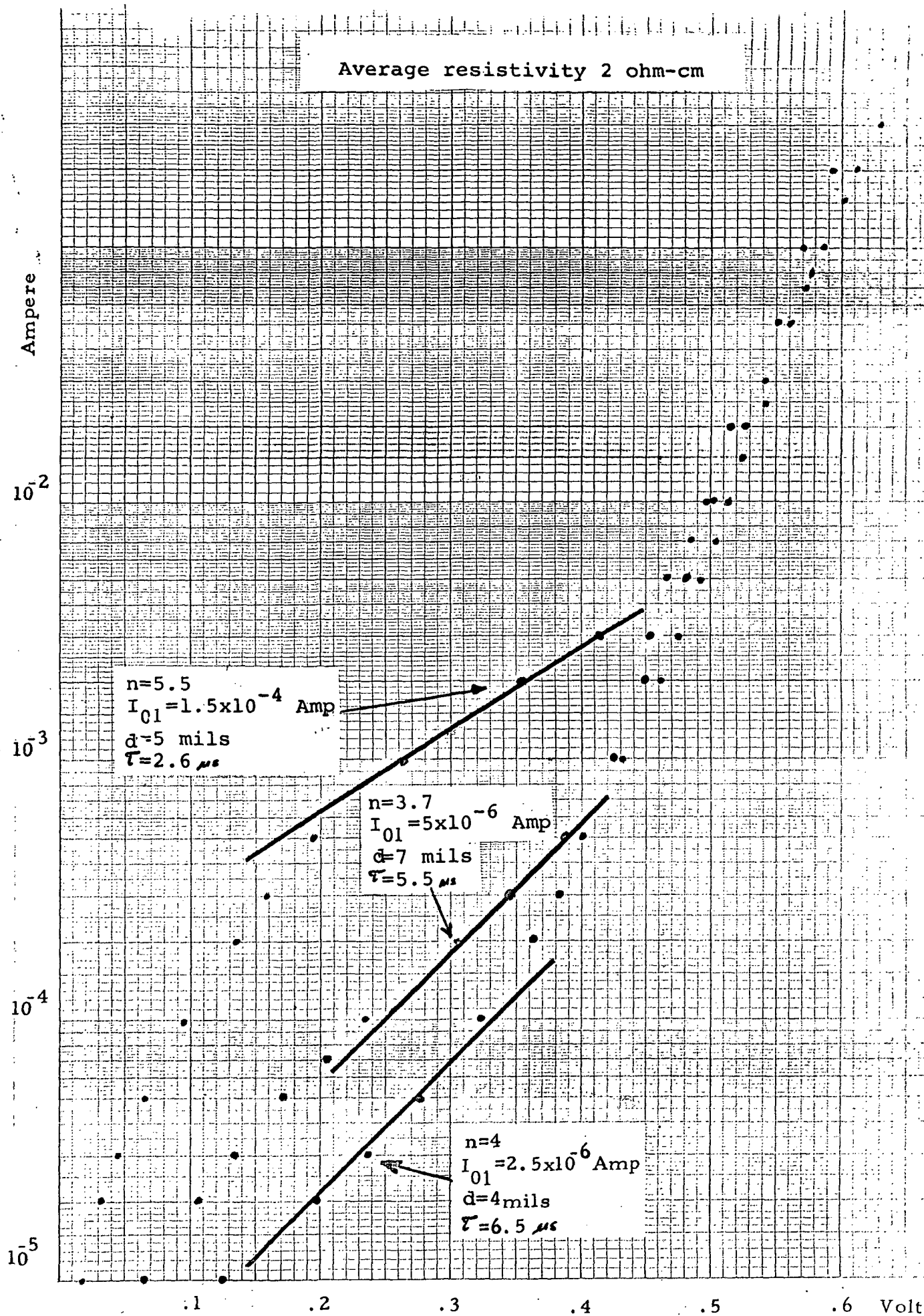


Figure 9. Representative dark I-V characteristics observed

efficiency at the front surface, dark-current characteristics, carrier lifetime near the front junction, and carrier lifetime near the rear high-low reflector junction. The optical coupling measurements were described above in Section E and we shall discuss here the electronic analysis measurements.

### 1. Voltage-Current Characteristics

Dark current in a solar cell can be expressed for our purposes as:

$$I = I_{01} [e^{qV/nkT} - 1] + I_{02} [e^{qV/kT} - 1]$$

The first term of this expression represents an excess current, and the second the ideal diffusion injection. It may be assumed that the excess current is associated with thermal generation sites in the depletion region. In room-temperature silicon  $I_{01} \gg I_{02}$ , which means that at low voltages the first term dominates, but above a moderate voltage the more rapidly rising second term becomes larger.

$I_{01}$  and  $n$  indicate the deviation of a given specimen from an ideal diode, and their measurement allows assessment of lattice damage associated with the front junction formation. The values of  $n$ ,  $I_{01}$  and  $I_{02}$  were determined from the slopes and intercepts of the dark  $\log I$  vs  $V$  characteristics for silicon cells having different resistivities and thicknesses. Figure 9. shows some of the dark  $I$ - $V$  characteristics for 2 ohm-cm cells of thickness 3, 5, 6 and 7 mils. Dark current plots for 0.2 ohm-cm cells having thicknesses of 10-12 mils were shown in Figure 4.



It was noted that there is a correlation between the magnitude of the excess current  $I_{01}$  observed for any particular cell and the value of the voltage multiplier in the exponent,  $n$ . Although the values of these two factors can be influenced by different crystal damage and surface mechanisms, there is a definite qualitative correlation in practice, as shown in Figure 10.

## 2. Injection Storage Lifetime

The measured dark capacitance of a p-n junction is the sum of the depletion layer capacitance and any diffusion capacitance. The diffusion capacitance represents charge storage in the form of injected excess minority carriers in transit. The charge stored is  $I \times \tau$ , where  $\tau$  is the lifetime of the injected minority carriers in the more lightly doped region if no ohmic contact is very close to the injecting junction.

The dark storage capacitance of injected minority carriers introduced in cells by forward bias was measured using a General Radio 1656 impedance bridge. For currents above  $5 \times 10^{-4}$  Ampere the dissipation factor was too high to allow accurate bridge balancing; therefore the capacitance was only measured up to  $1 \times 10^{-4}$  Amperes.

From these measurements the effective carrier lifetime could be determined, but since the storage capacitance was

(recombination current)

$$I = I_{01} (e^{qV/nkT} - 1) + I_{02} (e^{qV/kT} - 1)$$

$I_{01}$

$10^4$

$10^5$

$10^6$

$10^7$

1

2

3

4

5

$n$  (slope)

Figure 10.

Correspondence of extrapolated excess current and

measured at low current levels where  $I_{01} \gg I_{02}$ , it is to be expected that the lifetime values derived apply to the front depletion layer. Therefore, the storage capacitance measurement for low current levels mainly indicates how well a front junction was fabricated. Values derived from such measurements are also indicated on the log I vs V plots in Figure 4. and Figure 9.

### 3. Quantum Yield and Bulk Lifetime

The basic purpose of this measurement effort was to investigate a simple method for determining the effect of high-low junction formation on the effective minority carrier lifetime.

A spectrophotometer in the Solarex laboratories is normally used for measuring optical coupling properties as a function of wavelength. Since the instrument maintains a relatively constant input flux as a function of wavelength, it was used to indicate carrier losses near the back surface from the long-wavelength cell response.

Experimentally, the output of the cells exposed to a beam with a narrow spectrum band was used as the measurable parameter. The output at any particular wavelength was normalized to the photovoltage observed at 0.6 micron. These values were plotted on top of a reference yield versus wavelength

family of curves derived for a semi-infinite solid from which the minority carrier lifetime could be estimated, as in Figure 3. It is expected that the lifetime values derived apply to the deep bulk of the cell and that this measurement indicates the performance of the back junction electron reflector.